FORM PTO-1390 (REV. 11-2000) U S DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER	U.S. APPLICATION NO. (If known, see 37 CFR 1.5)
1163-0355P	09/936212

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/JP00/00682	February 8, 2000	- - - -

TITLE OF INVENTION

MULTISTAGE AMPLIFIER

APPLICANT(S) FOR DO/EO/US

MORI, Kazutomi; SHINJO, Shintarou; KITABAYASHI, Fumimasa; and IKEDA, Yukio

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39 (1).
4. ☐ The US has been elected by the expiration of 19 months from the priority date (Article 31).
5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   - a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
   - b. ☒ has been transmitted by the International Bureau. WO 01/59927
   - c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☒ An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   - a. ☒ is transmitted herewith.
   - b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4)
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3)).
   - a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   - b. ☐ have been transmitted by the International Bureau.
   - c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   - d. ☒ have not been made and will not be made.
8. ☐ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. ☐ An English language translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11. to 20. below concern document(s) or information included:

11. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98, Form PTO-1449(s), and International Search Report (PCT/ISA/210) with cited 5 document(s).
12. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☒ A FIRST preliminary amendment.
14. ☐ A SECOND or SUBSEQUENT preliminary amendment.
15. ☐ A substitute specification.
16. ☐ A change of power of attorney and/or address letter.
17. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821-1.825.
18. ☐ A second copy of the published international application under 35 U.S.C. 154(d)(4).
19. ☐ A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
20. ☒ Other items or information:
    1) Nine (9) Sheets of Formal Drawings

U.S. APPLICATION NO (if known, see 37 CFR 1.5)	INTERNATIONAL APPLICATION NO	ATTORNEY'S DOCKET NUMBER
09/936212 NEW	PCT/JP00/00682	1163-0355P

21. ☒ The following fees are submitted:	CALCULATIONS	PTO USE ONLY
BASIC NATIONAL FEE (37 CFR 1.492(a)(1)-(5):		
Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO. **$1,000.00**		
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO **$860.00**		
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO. **$710.00**		
International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4) **$690.00**		
International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4). **$100.00**		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$ 860.00	
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$ 0	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total Claims	8 - 20 =	0	X **$18.00**	$ 0	
Independent Claims	1 - 3 =	0	X **$80.00**	$ 0	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)		None	+ **$270.00**	$ 0	
		TOTAL OF ABOVE CALCULATIONS =		$ 860.00	
☐ Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by 1/2.				$ 0	
		SUBTOTAL =		$ 860.00	
Processing fee of **$130.00** for furnishing the English translation later than ☐20 ☐30 months from the earliest claimed priority date (37 CFR 1.492(f)). +				$ 0	
		TOTAL NATIONAL FEE =		$ 860.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property +				$ 40.00	
		TOTAL FEES ENCLOSED =		$ 900.00	
			Amount to be: refunded		$
			charged		$

a. ☒ A check in the amount of $ **900.00** to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account. No. _____ in the amount of $_____ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 02-2448.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

Send all correspondence to:
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Date: September 10, 2001

By _____
Michael K. Mutter, #29,680

MKM/jeb

PATENT
1163-0355P

IN THE U.S. PATENT AND TRADEMARK OFFICE

Applicant:	MORI et al.	Conf.:	Unknown
Appl. No.:	New	Group:	Unknown
Filed:	September 10, 2001	Examiner:	UNASSIGNED
For:	MULTISTAGE AMPLIFIER		

AMENDMENT

BOX PATENT APPLICATION
Assistant Commissioner for Patents
Washington, DC 20231

September 10, 2001

Sir:

The following preliminary Amendments and Remarks are respectfully submitted in connection with the above-identified application.

AMENDMENTS

Please amend the specification as follows:

Before line 1, insert

--This application is the national phase under 35 U.S.C. §371 of PCT International Application No. PCT/JP00/00682 which has an International filing date of February 8, 2000, which designated the United States of America.--

REMARKS

The specification has been amended to provide a cross-reference to the previously filed International Application.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

BIRCH, STEWART, KOLASCH & BIRCH, LLP

By _____
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1163-0355P

Attachment: Version with Markings to Show Changes Made

(Rev. 02/12/01)

Appl. No. New

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

The specification was amended to provide cross-referencing to the International Application.

SPECIFICATION

9/pts

TITLE OF THE INVENTION

MULTISTAGE AMPLIFIER

This application is the national phase under 35 U.S.C. § 371 of PCT International Application No. PCT/JP00/00682 which has an International filing date of February 8, 2000, which designated the United States of America and was not published in English.

TECHNICAL FIELD

The present invention relates to a multistage amplifier in which an input signal is amplified stage by stage and is output.

BACKGROUND ART

In a multistage amplifier using a type of semiconductor devices such as field effect transistors (FETs), bipolar junction transistors (BJTs) or hetero junction bipolar transistors (HBTs), an input matching circuit placed on an input side, an output matching circuit placed on an output side and an inter-stage matching circuit placed between the input matching circuit and the output matching circuit are generally arranged so as to bring out the performance of the type of semiconductor devices.

For example, Fig. 1 is a view of an equivalent circuit of a conventional multistage amplifier disclosed in "Technical Report of the Institute of Electronics, Information and Communication Engineers (IEICE), MW95-73", published in July of 1995. In Fig. 1, 1 indicates an input terminal for receiving a signal. 2 indicates an output terminal for outputting an amplified signal. 3 indicates a front-stage amplifying element for amplifying the signal received in the

input terminal 1. 4 indicates a rear-stage amplifying element for amplifying the signal amplified in the front-stage amplifying element 3.

5 indicates an input matching circuit of the conventional multistage amplifier. 6 indicates an inter-stage matching circuit for performing an impedance matching between the front-stage amplifying element 3 and the rear-stage amplifying element 4. 7 indicates a bias circuit. 8 indicates an output matching circuit of the conventional multistage amplifier. 9 indicates a short stub for bias supply. 10 indicates a parallel capacitor. 11 indicates a serial line. 12 indicates a serial capacitor.

Here, each of the front-stage amplifying element 3 and the rear-stage amplifying element 4 is composed of an FET, a BJT, a metal oxide semiconductor field effect transistor (MOSFET), a high electron mobility transistor (HEMT) or an HBT.

Next, an operation will be described below.

When a signal is received in the input terminal 1, the signal is sent to the front-stage amplifying element 3 through the input matching circuit 5, and the signal is amplified in the front-stage amplifying element 3.

Thereafter, the signal amplified in the front-stage amplifying element 3 is sent to the rear-stage amplifying element 4 through the inter-stage matching circuit 6 and the bias circuit 7, and the signal is amplified in the rear-stage amplifying element 4.

Thereafter, the signal amplified in the rear-stage amplifying element 4 is output from the output terminal 2 through the output matching circuit 8.

Here, a function of the inter-stage matching circuit 6 will be described below.

In the inter-stage matching circuit 6, an impedance matching is

performed on a certain reference plane between the front-stage amplifying element 3 and the rear-stage amplifying element 4 so as to make a pair of impedances conjugate to each other on both sides of the reference plane. Fig. 2 is an explanatory view showing a general example of matching conditions between the front-stage amplifying element 3 and the rear-stage amplifying element 4 of the conventional multistage amplifier.

As shown in Fig. 2, an output impedance of the front-stage amplifying element 3 is expressed by S_{Y_FET}, an impedance (that is, an output load impedance of the front-stage amplifying element 3) on an output side seen from the front-stage amplifying element 3 is expressed by F_{out}, an input impedance of the rear-stage amplifying element 4 is expressed by S_{X_FET}, an impedance (that is, an input source impedance of the rear-stage amplifying element 4) on an input side seen from the rear-stage amplifying element 4 is expressed by F_{in}.

In cases where a small signal operation is performed in the conventional multistage amplifier, an optimum output load impedance Γ_{opt_out} of the front-stage amplifying element 3 agrees with a conjugate complex impedance $S_{Y\_FET}^*$ of the output impedance S_{Y_FET} of the front-stage amplifying element 3, and an optimum input source impedance Γ_{opt_in} of the rear-stage amplifying element 4 agrees with a conjugate complex impedance $S_{X\_FET}^*$ of the input impedance S_{X_FET} of the rear-stage amplifying element 4.

Therefore, in cases where a conjugate complex impedance matching is performed at an output terminal X of the front-stage amplifying element 3, as shown in Fig. 2(b), the inter-stage matching circuit 6 is designed so as to perform an impedance transformation from the input impedance S_{X_FET} of the rear-stage amplifying element 4 to the conjugate complex impedance $S_{Y\_FET}^*$ ($=\Gamma_{opt\_out}$) of the output impedance S_{Y_FET} of the front-stage amplifying element 3.

Also, in cases where a conjugate complex impedance matching is performed at an input terminal Y of the rear-stage amplifying element 4, as shown in Fig. 2(c), the inter-stage matching circuit 6 is designed so as to perform an impedance transformation from the output impedance S_{Y_FET} of the front-stage amplifying element 3 to the conjugate complex impedance $S_{X\_FET}^*$ ($=\Gamma_{opt\_in}$) of the input impedance S_{X_FET} of the rear-stage amplifying element 4.

Therefore, in cases where no loss occurs in the inter-stage matching circuit 6, when the conjugate complex impedance matching is performed at the output terminal X of the front-stage amplifying element 3, the conjugate complex impedance matching can be performed at the input terminal Y of the rear-stage amplifying element 4 simultaneously with the conjugate complex impedance matching at the output terminal X.

However, a level of the input signal transmitted through the multistage amplifier induces the conventional multistage amplifier to perform a large signal operation in a final-stage amplifying element or an amplifying element just before the final-stage amplifying element of the conventional multistage amplifier in place of the small signal operation.

In this case, the output impedance S_{Y_FET} of the front-stage amplifying element 3 and the input impedance S_{X_FET} of the rear-stage amplifying element 4 in the large signal operation of the conventional multistage amplifier differ from those in the small signal operation, and optimum impedances, which maximize an efficiency of the conventional multistage amplifier, differ from the input and output impedances S_{X_FET} and S_{Y_FET}. Therefore, in the large signal operation, the optimum output load impedance Γ_{opt_out} of the front-stage amplifying element 3 differs from the conjugate complex impedance $S_{Y\_FET}^*$ of the output impedance S_{Y_FET} of the front-stage amplifying element 3, and the optimum input source impedance Γ_{opt_in} of the rear-stage amplifying element 4

differs from the conjugate complex impedance $S_{X\_FET}^*$ of the input impedance S_{X_FET} of the rear-stage amplifying element 4.

Therefore, in cases where a conjugate complex impedance matching is performed at the output terminal X of the front-stage amplifying element 3, as shown in Fig. 2(b), the inter-stage matching circuit 6 is designed so as to perform an impedance transformation from the input impedance S_{X_FET} of the rear-stage amplifying element 4 to the optimum output load impedance Γ_{opt_out} ($\neq S_{Y\_FET}^*$) of the front-stage amplifying element 3. Also, in cases where a conjugate complex impedance matching is performed at the input terminal Y of the rear-stage amplifying element 4, as shown in Fig. 2(c), the inter-stage matching circuit 6 is designed so as to perform an impedance transformation from the output impedance S_{Y_FET} of the front-stage amplifying element 3 to the optimum input source impedance Γ_{opt_in} ($\neq S_{X\_FET}^*$) of the rear-stage amplifying element 4.

In this case, it is impossible for the inter-stage matching circuit 6 to perform the conjugate complex impedance matching at the output terminal X of the front-stage amplifying element 3 simultaneously with the conjugate complex impedance matching at the input terminal Y of the rear-stage amplifying element 4.

Because the conventional multistage amplifier has the above described configuration, it is impossible to perform the matching of the output load impedance F_{out} of the front-stage amplifying element 3 with the optimum output load impedance Γ_{opt_out} simultaneously with the matching of the input source impedance F_{in} of the rear-stage amplifying element 4 with the optimum input source impedance Γ_{opt_in}. Therefore, a problem has arisen that an efficiency of the whole conventional multistage amplifier is lowered.

The present invention is provided to solve the above-described problem, and the object of the present invention is to provide a

multistage amplifier in which an output load impedance of a front-stage amplifying element and an input source impedance of a rear-stage amplifying element are simultaneously matched with optimum impedances respectively.

DISCLOSURE OF THE INVENTION

A multistage amplifier according to the present invention has a matching circuit comprising a one-stage high pass filter type matching unit and a one-stage low pass filter type matching unit serially connected with the one-stage high pass filter type matching unit.

Therefore, because an output load impedance of a front-stage amplifying element and an input source impedance of a rear-stage amplifying element can be matched with the optimum impedances respectively, an efficiency of the whole multistage amplifier can be heightened.

In the multistage amplifier according to the present invention, the matching circuit arranged between the final-stage amplifying element and the amplifying element placed just before the final-stage amplifying element comprises the one-stage high pass filter type matching unit and the one-stage low pass filter type matching unit serially connected with each other.

Therefore, a small-sized multistage amplifier can be obtained.

In the multistage amplifier according to the present invention, the one-stage high pass filter type matching unit is placed on an input side of the input signal, and the one-stage low pass filter type matching unit is placed on an output side of the amplified signal.

Therefore, an output load impedance of a front-stage amplifying element and an input source impedance of a rear-stage amplifying element can be matched with the optimum impedances respectively.

In the multistage amplifier according to the present invention, the

one-stage low pass filter type matching unit is placed on an input side of the input signal, and the one-stage high pass filter type matching unit is placed on an output side of the amplified signal.

Therefore, an output load impedance of a front-stage amplifying element and an input source impedance of a rear-stage amplifying element can be matched with the optimum impedances respectively.

In the multistage amplifier according to the present invention, the one-stage high pass filter type matching unit comprises a parallel inductor and a serial capacitor.

Therefore, a small-sized one-stage high pass filter type matching unit can be obtained.

In the multistage amplifier according to the present invention, a bias supply short stub having a length equal to or shorter than 1/4 of a wavelength of the input signal is used as the parallel inductor.

Therefore, because the bias supply short stub can be used as a bias supply line on an output side of the front-stage amplifying element, a small-sized multistage amplifier can be obtained.

In the multistage amplifier according to the present invention, the one-stage low pass filter type matching unit comprises a parallel capacitor and a serial inductor.

Therefore, a small-sized one-stage low pass filter type matching unit can be obtained.

In the multistage amplifier according to the present invention, a serial line is used as the serial inductor.

Therefore, a small-sized one-stage low pass filter type matching unit can be obtained.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a view of an equivalent circuit of a conventional multistage amplifier.

Fig. 2 is an explanatory view showing a general example of matching conditions between a front-stage amplifying element and a rear-stage amplifying element of the conventional multistage amplifier.

Fig. 3 is a view of an equivalent circuit of a multistage amplifier according to a first embodiment of the present invention.

Fig. 4 is an explanatory view showing an optimum output load impedance of a front-stage amplifying element and an optimum input source impedance of a rear-stage amplifying element.

Fig. 5 is an explanatory view showing impedances between a front-stage amplifying element and a rear-stage amplifying element in cases where an inter-stage matching circuit comprises a one-stage high pass filter type matching unit and a one-stage low pass filter type matching unit.

Fig. 6 is a view of an equivalent circuit of a multistage amplifier according to a second embodiment of the present invention.

Fig. 7 is an explanatory view showing impedances in an inter-stage matching circuit in cases where the inter-stage matching circuit comprises a one-stage low pass filter type matching unit and a one-stage high pass filter type matching unit.

Fig. 8 is a view of an equivalent circuit of a multistage amplifier according to a third embodiment of the present invention.

Fig. 9 is a view of an equivalent circuit of a multistage amplifier according to a fourth embodiment of the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

Hereinafter, the best mode for carrying out the present invention will now be described with reference to the accompanying drawings to explain the present invention in more detail.

EMBODIMENT 1

Fig. 3 is a view of an equivalent circuit of a multistage amplifier

according to a first embodiment of the present invention.

In Fig. 3, 21 indicates an input terminal for receiving a signal. 22 indicates an output terminal for outputting an amplified signal. 23 indicates a front-stage amplifying element for amplifying the signal received in the input terminal 21. 24 indicates a rear-stage amplifying element for amplifying the signal amplified in the front-stage amplifying element 23.

25 indicates an input matching circuit of the multistage amplifier. 26 indicates an inter-stage matching circuit for performing an impedance matching between the front-stage amplifying element 23 and the rear-stage amplifying element 24. 27 indicates an output matching circuit of the multistage amplifier. 28 indicates a one-stage high pass filter type matching unit of the inter-stage matching circuit 26. 29 indicates a one-stage low pass filter type matching unit of the inter-stage matching circuit 26.

31 indicates a parallel inductor of the one-stage high pass filter type matching unit 28. 32 indicates a serial capacitor of the one-stage high pass filter type matching unit 28. 33 indicates a parallel capacitor of the one-stage low pass filter type matching unit 29. 34 indicates a serial inductor of the one-stage low pass filter type matching unit 29.

Here, each of the front-stage amplifying element 23 and the rear-stage amplifying element 24 is composed of an FET, a BJT, an MOSFET, an HEMT or an HBT.

Next, an operation of the multistage amplifier will be described below.

When a signal is received in the input terminal 21, the signal is sent to the front-stage amplifying element 23 through the input matching circuit 25, and the signal is amplified in the front-stage amplifying element 23.

Thereafter, the signal amplified in the front-stage amplifying element 23 is sent to the rear-stage amplifying element 24 through the inter-stage matching circuit 26 comprising the one-stage high pass filter type matching unit 28 and the one-stage low pass filter type matching unit 29, and the signal is amplified in the rear-stage amplifying element 24.

Thereafter, the signal amplified in the rear-stage amplifying element 24 is output from the output terminal 22 through the output matching circuit 27.

Here, a high electron mobility transistor (HEMT) element having a gate width of 5.8 mm is, for example, used as the front-stage amplifying element 23, an optimum output load impedance Γ_{opt_out} of the HEMT element and a conjugate complex impedance S_{Y_FET}* of an output impedance of the HEMT element are shown in Fig. 4(a).

Also, a high electron mobility transistor (HEMT) element having a gate width of 17.5 mm is, for example, used as the rear-stage amplifying element 24, an optimum input source impedance Γ_{opt_in} of the HEMT element and a conjugate complex impedance S_{X_FET}* of an input impedance of the HEMT element are shown in Fig. 4(b).

Bias conditions for the HEMT elements are Class-AB together. In this case, the gate width of the front-stage amplifying element 23 is equal to or lower than a half of the gate width of the rear-stage amplifying element 24.

The optimum input source impedance Γ_{opt_in} of the rear-stage amplifying element 24 (the HEMT element of the gate width of 17.5 mm) corresponds to an impedance, at which a maximum efficiency is obtained in the multistage amplifier, in cases where a prescribed distortion condition is satisfied at an output electric power level of almost 3 dB in back off, and the optimum input source impedance Γ_{opt_in} is determined by performing load-pull and source-pull measurements.

The optimum output load impedance Γ_{opt_out} of the front-stage amplifying element 23 (the HEMT element of the gate width of 5.8 mm) is determined by examining various combinations of characteristics of the front-stage amplifying element 23 and the rear-stage amplifying element 24 according to both a result of load-pull and source-pull measurements for the HEMT element of the gate width of 5.8 mm and the result of the load-pull and source-pull measurements for the HEMT element of the gate width of 17.5 mm, determining a specific combination of characteristics of the front-stage amplifying element 23 and the rear-stage amplifying element 24 on condition that a maximum efficiency in the multistage amplifier is obtained in cases where a prescribed distortion condition is satisfied as a two-stage amplifier at an output electric power level of almost 3 dB in back off and adopting an output load impedance of the front-stage amplifying element 23 determined in the specific combination as the optimum output load impedance Γ_{opt_out}.

As shown in Fig. 4(a), a real part of the optimum output load impedance Γ_{opt_out} of the front-stage amplifying element 23 (the HEMT element of the gate width of 5.8 mm) is moved toward a low impedance direction as compared with the conjugate complex impedance S_{Y_FET}* of the output impedance of the front-stage amplifying element 23, and an imaginary part of the optimum output load impedance Γ_{opt_out} of the front-stage amplifying element 23 is moved toward an inductive direction as compared with the conjugate complex impedance S_{Y_FET}* of the output impedance of the front-stage amplifying element 23.

Also, as shown in Fig. 4(b), a real part of the optimum input source impedance Γ_{opt_in} of the rear-stage amplifying element 24 (the HEMT element of the gate width of 17.5 mm) is moved toward a high impedance direction as compared with the conjugate complex impedance S_{X_FET}* of the input impedance of the rear-stage amplifying element 24, and an

imaginary part of the optimum input source impedance Γ_{opt_in} of the rear-stage amplifying element 24 is moved toward an inductive direction as compared with the conjugate complex impedance $S_{X\_FET}^*$ of the input impedance of the rear-stage amplifying element 24.

Next, an output load impedance Γ_{out} of the front-stage amplifying element 23 and an input source impedance Γ_{in} of the rear-stage amplifying element 24 are shown in Fig. 5 in cases where the inter-stage matching circuit 26 comprising the one-stage high pass filter type matching unit 28 and the one-stage low pass filter type matching unit 29 is used for the multistage amplifier.

In Fig. 5(a) and Fig. 5(b), impedances designated by symbols ◆ indicate the conjugate complex impedance $S_{Y\_FET}^*$ of the output impedance of the front-stage amplifying element 23 and the conjugate complex impedance $S_{X\_FET}^*$ of the input impedance of the rear-stage amplifying element 24 respectively, an area enclosed by a dotted circle in Fig. 5(a) indicates a neighboring area of the optimum output load impedance Γ_{opt_out} shown in Fig. 4(a), and an area enclosed by a dotted circle in Fig. 5(b) indicates a neighboring area of the optimum input source impedance Γ_{opt_in} shown in Fig. 4(b).

Here, in cases where the inter-stage matching circuit 26 comprising the one-stage high pass filter type matching unit 28 and the one-stage low pass filter type matching unit 29 is used for the multistage amplifier, the output load impedance Γ_{out} of the front-stage amplifying element 23 is examined when the input source impedance Γ_{in} of the rear-stage amplifying element 24 is matched with an impedance differing from the conjugate complex impedance $S_{X\_FET}^*$ of the input impedance of the rear-stage amplifying element 24.

For example, in cases where the inter-stage matching circuit 26 is arranged in the multistage amplifier so as to match the input source impedance Γ_{in} of the rear-stage amplifying element 24 with an impedance

indicated by an "A" symbol ● of Fig. 5(b), the output load impedance Γ_{out} of the front-stage amplifying element 23 is set to an impedance indicated by an "A" symbol ● of Fig. 5(a).

Also, in the same manner as the example of the impedance indicated by the "A" symbol ●, the output load impedance Γ_{out} of the front-stage amplifying element 23 is set to an impedance indicated by each of the "B" to "H" symbols ● of Fig. 5(a) when the input source impedance Γ_{in} of the rear-stage amplifying element 24 is matched with an impedance indicated by the corresponding symbol ● of Fig. 5(b).

As is described above, when the input source impedance Γ_{in} of the rear-stage amplifying element 24 is matched with the impedance of each of the "A" to "H" symbols ● placed on a circle in Fig. 5(b), the output load impedance Γ_{out} of the front-stage amplifying element 23 is set to the impedance of the corresponding symbol selected from the "A" to "H" symbols ● placed on a circle in Fig. 5(a). In particular, in case of the impedance of the "B" symbol ●, as shown in Fig. 5(a) and Fig. 5(b), the input source impedance Γ_{in} of the rear-stage amplifying element 24 is placed in the neighboring area of the optimum input source impedance Γ_{opt_in} of the rear-stage amplifying element 24, and the output load impedance Γ_{out} of the front-stage amplifying element 23 is placed in the neighboring area of the optimum output load impedance Γ_{opt_out} of the front-stage amplifying element 23.

Accordingly, in cases where the inter-stage matching circuit 26 comprises the one-stage high pass filter type matching unit 28 and the one-stage low pass filter type matching unit 29, the output load impedance Γ_{out} of the front-stage amplifying element 23 can almost agree with the optimum output load impedance Γ_{opt_out}, and the input source impedance Γ_{in} of the rear-stage amplifying element 24 can almost agree with the optimum input source impedance Γ_{opt_in}.

Therefore, because an inter-stage matching condition of the

multistage amplifier can be further optimized, the efficiency of the whole multistage amplifier can be heightened.

Here, assuming that the inter-stage matching circuit 26 has only a one-stage low pass filter type matching unit, a one-stage high pass filter type matching unit, a two-stage low pass filter type matching unit or a two-stage high pass filter type matching unit, even though the inter-stage matching circuit 26 is arranged in the multistage amplifier so as to match the input source impedance Γ_{in} of the rear-stage amplifying element 24 with the impedance of the "B" symbol ● placed in the neighboring area of the optimum input source impedance Γ_{opt_in}, the output load impedance Γ_{out} of the front-stage amplifying element 23 is set to an impedance considerably differing from the impedance of the "B" symbol ● shown in Fig. 5(a). Therefore, the output load impedance Γ_{out} of the front-stage amplifying element 23 cannot agree with the optimum output load impedance Γ_{opt_out}. Also, in the same manner, the input source impedance Γ_{in} of the rear-stage amplifying element 24 cannot agree with the optimum input source impedance Γ_{opt_in}.

In case of the prior art shown in Fig. 1, to exert no influence of the short tub 9 or the serial capacitor 12 on the impedances at an operation frequency of the input signal, the short tub 9 for bias supply has a length near to 1/4 of a wavelength of the input signal, and the serial capacitor 12 has a sufficiently high capacitance. Therefore, the inter-stage matching circuit 6 substantially composed of the parallel capacitor 10 and the serial line 11 functions as one-stage low pass filter type matching unit. Accordingly, the output load impedance Γ_{out} of the front-stage amplifying element 3 cannot agree with the optimum output load impedance Γ_{opt_out}, and the input source impedance Γ_{in} of the rear-stage amplifying element 4 cannot agree with the optimum input source impedance Γ_{opt_in}.

In the first embodiment, the multistage amplifier corresponding to two stages (the front-stage amplifying element 23 and the rear-stage amplifying element 24) is described. However, it is applicable that the multistage amplifier have three stages or more. In case of the multistage amplifier having three stages or more, an inter-stage matching circuit 26 (hereinafter, called a final inter-stage matching circuit) between an amplifying element of a final stage and an amplifying element of a stage just before the final stage comprises the one-stage high pass filter type matching unit 28 and the one-stage low pass filter type matching unit 29. In this case, even though an inter-stage matching circuit existing in the input-side direction from the final inter-stage matching circuit 26 does not have both the one-stage high pass filter type matching unit 28 and the one-stage low pass filter type matching unit 29, the same effect as that of the first embodiment can be obtained in the multistage amplifier having three stages or more.

Therefore, because a small-sized matching circuit such as a one-stage low pass filter type matching unit can be used as an inter-stage matching circuit existing in the input-side direction from the final inter-stage matching circuit 26, a small-sized multistage amplifier can be obtained.

EMBODIMENT 2

Fig. 6 is a view of an equivalent circuit of a multistage amplifier according to a second embodiment of the present invention. In Fig. 6, the constituent elements, which are the same as or equivalent to those shown in Fig. 3, are indicated by the same reference numerals as those of the constituent elements shown in Fig. 3, and additional description of those constituent elements is omitted.

41 indicates an inter-stage matching circuit for performing an

impedance matching between the front-stage amplifying element 23 and the rear-stage amplifying element 24. 42 indicates a one-stage low pass filter type matching unit of the inter-stage matching circuit 41. 43 indicates a one-stage high pass filter type matching unit of the inter-stage matching circuit 41.

44 indicates a parallel capacitor of the one-stage low pass filter type matching unit 42. 45 indicates a serial inductor of the one-stage low pass filter type matching unit 42. 46 indicates a parallel inductor of the one-stage high pass filter type matching unit 43. 47 indicates a serial capacitor of the one-stage high pass filter type matching unit 43.

Next, an operation of the multistage amplifier will be described below.

In the first embodiment, the inter-stage matching circuit 26 comprises the one-stage high pass filter type matching unit 28 arranged on the input side and the one-stage low pass filter type matching unit 29 arranged on the output side. However, in the second embodiment, the inter-stage matching circuit 41 comprises the one-stage low pass filter type matching unit 42 arranged on the input side and the one-stage high pass filter type matching unit 43 arranged on the output side. The inter-stage matching circuit 41 will be described below in detail.

An output load impedance Γ_{out} of the front-stage amplifying element 23 and an input source impedance Γ_{in} of the rear-stage amplifying element 24 are shown in Fig. 7 in cases where the inter-stage matching circuit 41 comprising the one-stage low pass filter type matching unit 42 and the one-stage high pass filter type matching unit 43 is used for the multistage amplifier.

In Fig. 7(a) and Fig. 7(b), impedances designated by symbols ◆ indicate the conjugate complex impedance $S_{Y\_FET}^*$ of the output impedance

of the front-stage amplifying element 23 and the conjugate complex impedance $S_{X\_FET}^*$ of the input impedance of the rear-stage amplifying element 24 respectively, an area enclosed by a dotted circle in Fig. 7(a) indicates a neighboring area of the optimum output load impedance Γ_{opt_out} shown in Fig. 4(a), and an area enclosed by a dotted circle in Fig. 7(b) indicates a neighboring area of the optimum input source impedance Γ_{opt_in} shown in Fig. 4(b).

Here, in cases where the inter-stage matching circuit 41 comprising the one-stage low pass filter type matching unit 42 and the one-stage high pass filter type matching unit 43 is used for the multistage amplifier, the output load impedance Γ_{out} of the front-stage amplifying element 23 is examined when the input source impedance Γ_{in} of the rear-stage amplifying element 24 is matched with an impedance differing from the conjugate complex impedance $S_{X\_FET}^*$ of the input impedance of the rear-stage amplifying element 24.

For example, in cases where the inter-stage matching circuit 41 is arranged in the multistage amplifier so as to match the input source impedance Γ_{in} of the rear-stage amplifying element 24 with an impedance indicated by an "A" symbol ● of Fig. 7(b), the output load impedance Γ_{out} of the front-stage amplifying element 23 is set to an impedance indicated by an "A" symbol ● of Fig. 7(a).

Also, in the same manner as the example of the impedance indicated by the "A" symbol ●, the output load impedance Γ_{out} of the front-stage amplifying element 23 is set to an impedance indicated by each of the "B" to "H" symbols ● of Fig. 7(a) when the input source impedance Γ_{in} of the rear-stage amplifying element 24 is matched with an impedance indicated by the corresponding symbol ● of Fig. 7(b).

As is described above, when the input source impedance Γ_{in} of the rear-stage amplifying element 24 is matched with the impedance of each of the "A" to "H" symbols ● placed on a circle in Fig. 7(b), the output

load impedance Γ_{out} of the front-stage amplifying element 23 is set to the impedance of the corresponding symbol selected from the "A" to "H" symbols ● placed on a circle in Fig. 7(a). In particular, in case of the impedance of the "B" symbol ●, as shown in Fig. 5(a) and Fig. 5(b), the input source impedance Γ_{in} of the rear-stage amplifying element 24 is placed in the neighboring area of the optimum input source impedance Γ_{opt_in} of the rear-stage amplifying element 24, and the output load impedance Γ_{out} of the front-stage amplifying element 23 is placed in the neighboring area of the optimum output load impedance Γ_{opt_out} of the front-stage amplifying element 23.

Accordingly, in cases where the inter-stage matching circuit 41 comprises the one-stage low pass filter type matching unit 42 and the one-stage high pass filter type matching unit 43, the output load impedance Γ_{out} of the front-stage amplifying element 23 can almost agree with the optimum output load impedance Γ_{opt_out}, and the input source impedance Γ_{in} of the rear-stage amplifying element 24 can almost agree with the optimum input source impedance Γ_{opt_in}.

Therefore, because an inter-stage matching condition of the multistage amplifier can be further optimized, the efficiency of the whole multistage amplifier can be heightened.

EMBODIMENT 3

Fig. 8 is a view of an equivalent circuit of a multistage amplifier according to a third embodiment of the present invention. In Fig. 8, the constituent elements, which are the same as or equivalent to those shown in Fig. 3, are indicated by the same reference numerals as those of the constituent elements shown in Fig. 3, and additional description of those constituent elements is omitted.

51 indicates a bias supply short stub of the one-stage high pass filter type matching unit 28. A length of the bias supply short stub

51 is equal to or shorter than 1/4 of a wavelength of the signal. 52 indicates a serial line of the one-stage low pass filter type matching unit 29.

Next, an operation of the multistage amplifier will be described below.

In the first embodiment, the one-stage high pass filter type matching unit 28 comprises the parallel inductor 31 and the serial capacitor 32, and the one-stage low pass filter type matching unit 29 comprises the parallel capacitor 33 and the serial inductor 34. However, in the third embodiment, the one-stage high pass filter type matching unit 28 comprises the bias supply short stub 51 having the length equal to or shorter than 1/4 of the wavelength of the signal in place of the parallel inductor 31, and the one-stage low pass filter type matching unit 29 comprises the serial line 52 in place of the serial inductor 34.

In cases where a parallel short stub has a length equal to or shorter than 1/4 of the wavelength of the signal, the parallel short stub has the same electric characteristic as that of a parallel inductor. Also, a serial line has the same electric characteristic as that of a serial inductor.

Accordingly, because the inter-stage matching circuit 26 of the multistage amplifier comprises the one-stage high pass filter type matching unit 28 having the bias supply short stub 51 and the one-stage low pass filter type matching unit 29 having the serial line 52, the output load impedance Γ_{out} of the front-stage amplifying element 23 can almost agree with the optimum output load impedance Γ_{opt_out}, and the input source impedance Γ_{in} of the rear-stage amplifying element 24 can almost agree with the optimum input source impedance Γ_{opt_in}.

Therefore, because an inter-stage matching condition of the multistage amplifier can be further optimized, the efficiency of the

whole multistage amplifier can be heightened.

Also, because the one-stage high pass filter type matching unit 28 comprises the bias supply short stub 51 having the length equal to or shorter than 1/4 of the wavelength of the signal in place of the parallel inductor 31, the bias supply short stub 51 can be used as a bias supply line placed on the output side of the front-stage amplifying element 23. Therefore, a small-sized multistage amplifier can be obtained.

EMBODIMENT 4

Fig. 9 is a view of an equivalent circuit of a multistage amplifier according to a fourth embodiment of the present invention. In Fig. 9, the constituent elements, which are the same as or equivalent to those shown in Fig. 6, are indicated by the same reference numerals as those of the constituent elements shown in Fig. 6, and additional description of those constituent elements is omitted.

61 indicates a serial line of the one-stage low pass filter type matching unit 42. 62 indicates a bias supply short stub of the one-stage high pass filter type matching unit 43. A length of the bias supply short stub 62 is equal to or shorter than 1/4 of the wavelength of the signal.

Next, an operation of the multistage amplifier will be described below.

In the second embodiment, the one-stage low pass filter type matching unit 42 comprises the parallel capacitor 44 and the serial inductor 45, and the one-stage high pass filter type matching unit 43 comprises the parallel inductor 46 and the serial capacitor 47. However, in the fourth embodiment, the one-stage low pass filter type matching unit 42 comprises the serial line 61 in place of the serial inductor 45, and the one-stage high pass filter type matching unit 43 comprises

the bias supply short stub 62 having the length equal to or shorter than 1/4 of the wavelength of the signal in place of the parallel inductor 46.

A serial line has the same electric characteristic as that of a serial inductor. Also, in cases where a parallel short stub has a length equal to or shorter than 1/4 of a wavelength of a signal, the parallel short stub has the same electric characteristic as that of a parallel inductor.

Accordingly, because the inter-stage matching circuit 26 of the multistage amplifier comprises the one-stage low pass filter type matching unit 42 having the serial line 61 and the one-stage high pass filter type matching unit 43 having the bias supply short stub 62, the output load impedance Γ_{out} of the front-stage amplifying element 23 can almost agree with the optimum output load impedance Γ_{opt_out}, and the input source impedance Γ_{in} of the rear-stage amplifying element 24 can almost agree with the optimum input source impedance Γ_{opt_in}.

Therefore, because an inter-stage matching condition of the multistage amplifier can be further optimized, the efficiency of the whole multistage amplifier can be heightened.

Also, because the one-stage high pass filter type matching unit 43 comprises the bias supply short stub 62 having the length equal to or shorter than 1/4 of the wavelength of the signal in place of the parallel inductor 46, the bias supply short stub 62 can be used as a bias supply line placed on the output side of the front-stage amplifying element 23. Therefore, a small-sized multistage amplifier can be obtained.

INDUSTRIAL APPLICABILITY

As is described above, in cases where satellite communication, terrestrial microwave communication or mobile communication is performed, the multistage amplifier according to the present invention is appropriate to amplify a transmission signal or a receiving signal.

WHAT IS CLAIMED IS:

1. A multistage amplifier, comprising:

a plurality of amplifying elements for amplifying an input signal stage by stage and outputting an amplified signal; and

a matching circuit, arranged between each pair of amplifying elements adjacent to each other, for performing an impedance matching between the pair of amplifying elements,

characterized in that one matching circuit comprises:

a one-stage high pass filter type matching unit; and

a one-stage low pass filter type matching unit serially connected with the one-stage high pass filter type matching unit.

2. A multistage amplifier according to claim 1, wherein the matching circuit arranged between the final-stage amplifying element and the amplifying element placed just before the final-stage amplifying element comprises the one-stage high pass filter type matching unit and the one-stage low pass filter type matching unit serially connected with each other.

3. A multistage amplifier according to claim 1, wherein the one-stage high pass filter type matching unit is placed on an input side of the input signal, and the one-stage low pass filter type matching unit is placed on an output side of the amplified signal.

4. A multistage amplifier according to claim 1, wherein the one-stage low pass filter type matching unit is placed on an input side of the input signal, and the one-stage high pass filter type matching unit is placed on an output side of the amplified signal.

5. A multistage amplifier according to claim 1, wherein the one-

stage high pass filter type matching unit comprises a parallel inductor and a serial capacitor.

6. A multistage amplifier according to claim 5, wherein a bias supply short stub having a length equal to or shorter than 1/4 of a wavelength of the input signal is used as the parallel inductor.

7. A multistage amplifier according to claim 1, wherein the one-stage low pass filter type matching unit comprises a parallel capacitor and a serial inductor.

8. A multistage amplifier according to claim 7, wherein a serial line is used as the serial inductor.

ABSTRACT OF THE DISCLOSURE

An inter-stage matching circuit 26 comprises a one-stage high pass filter type matching unit 28 and a one-stage low pass filter type matching unit 29 serially connected with each other.

FIG.1

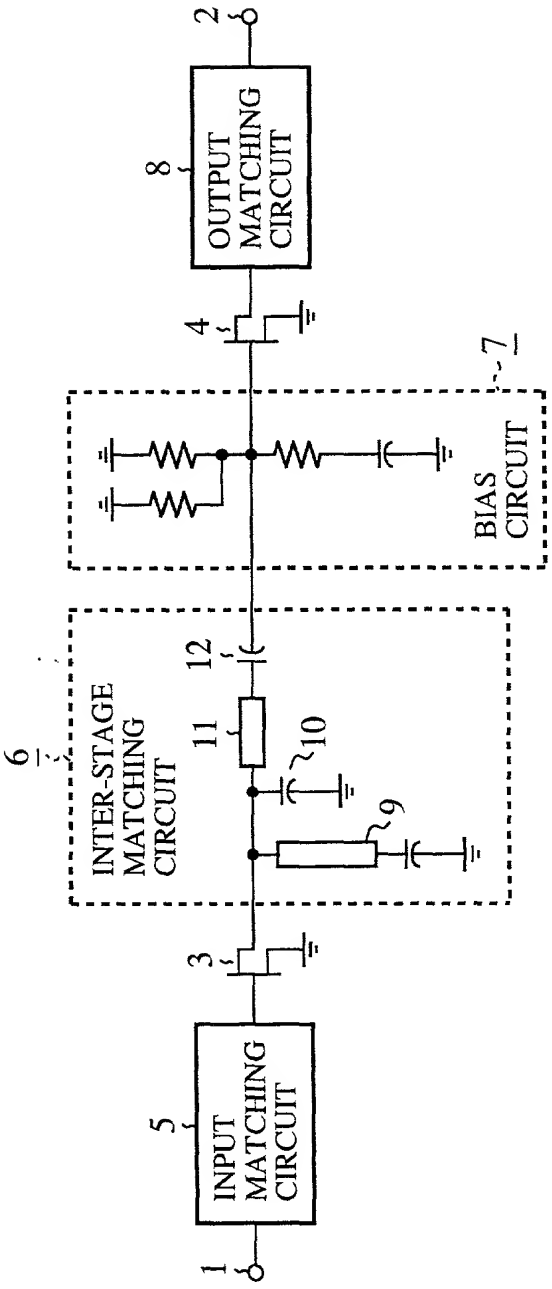

1
2
3
4
5
6
7
8
9
10
11
12
INPUT MATCHING CIRCUIT
OUTPUT MATCHING CIRCUIT
INTER-STAGE MATCHING CIRCUIT
BIAS CIRCUIT

FIG.2

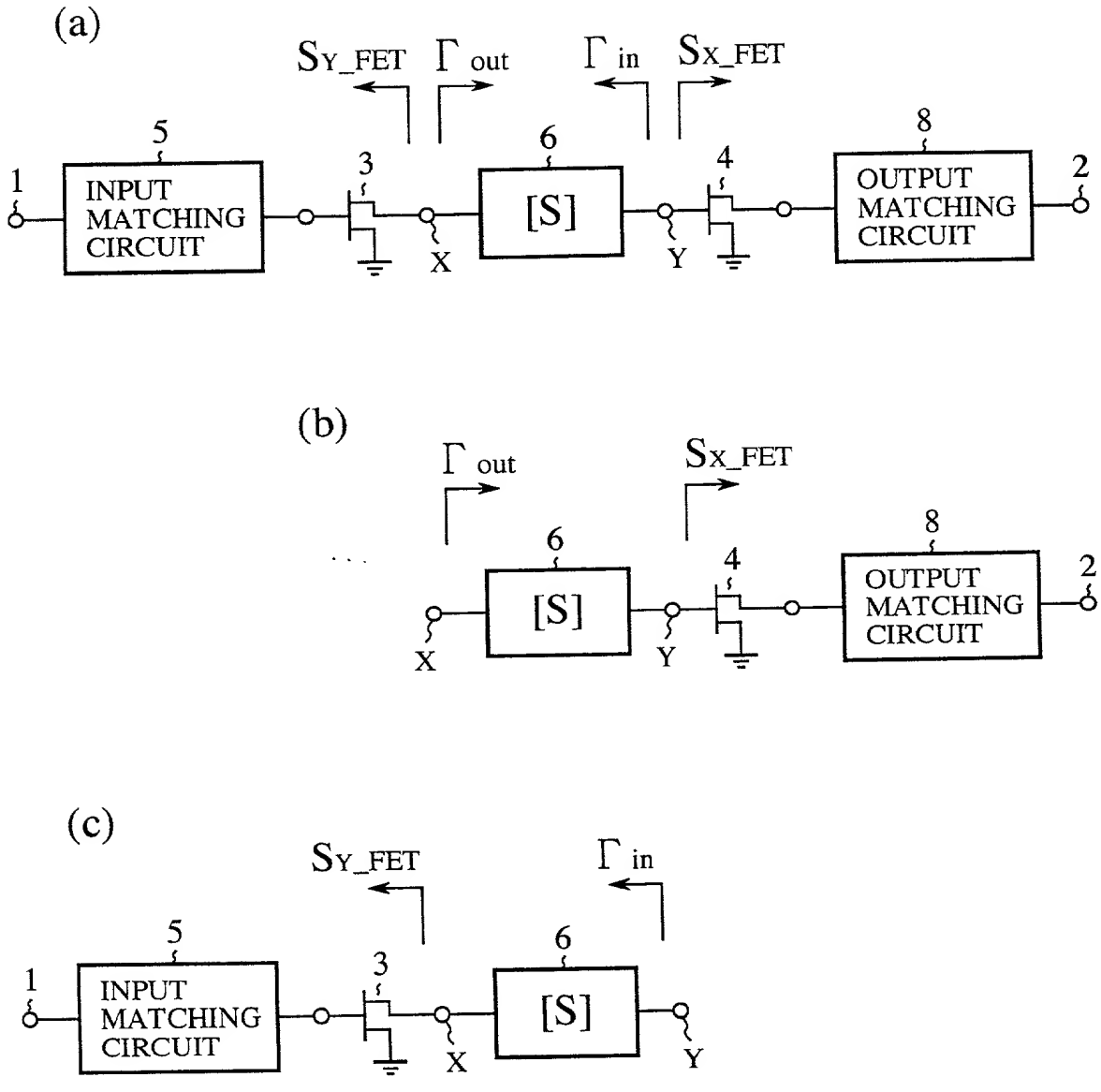

(a)
SY_FET
Γ out
Γ in
SX_FET
5
6
8
1
3
4
2
INPUT MATCHING CIRCUIT
[S]
OUTPUT MATCHING CIRCUIT
X
Y
(b)
Γ out
SX_FET
6
8
4
2
[S]
OUTPUT MATCHING CIRCUIT
X
Y
(c)
SY_FET
Γ in
5
6
1
3
INPUT MATCHING CIRCUIT
[S]
X
Y

FIG.3

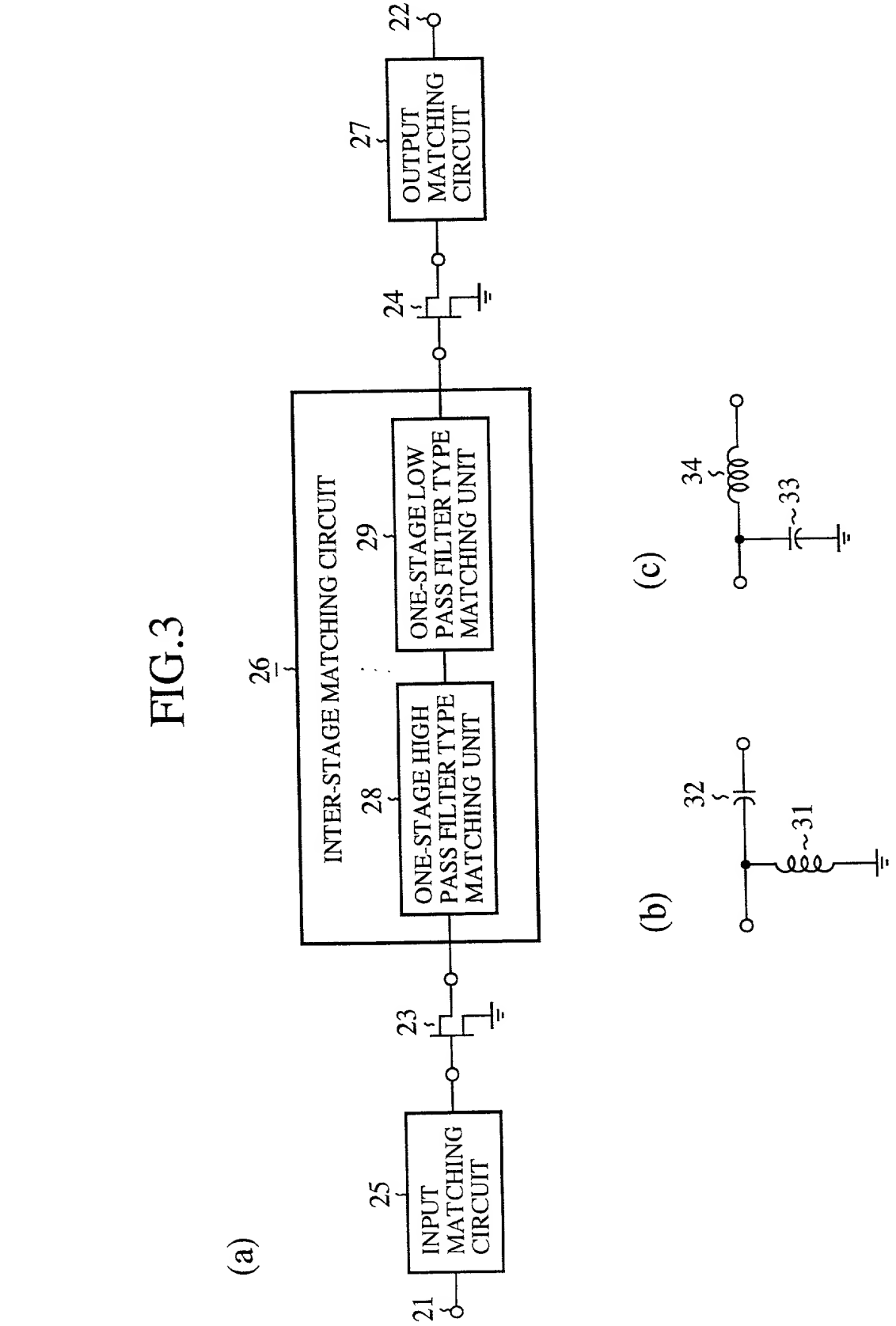

(a)
21
25
INPUT MATCHING CIRCUIT
23
26
INTER-STAGE MATCHING CIRCUIT
28
ONE-STAGE HIGH PASS FILTER TYPE MATCHING UNIT
29
ONE-STAGE LOW PASS FILTER TYPE MATCHING UNIT
24
27
OUTPUT MATCHING CIRCUIT
22
(b)
32
31
(c)
34
33

FIG.4

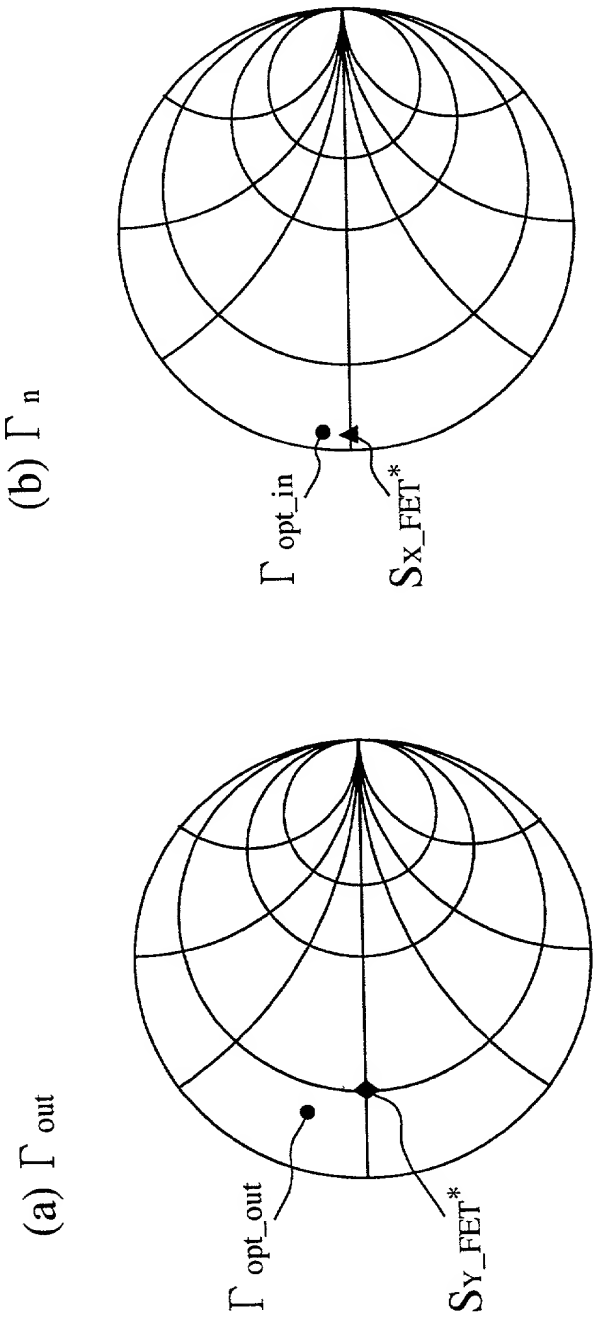


FIG.5

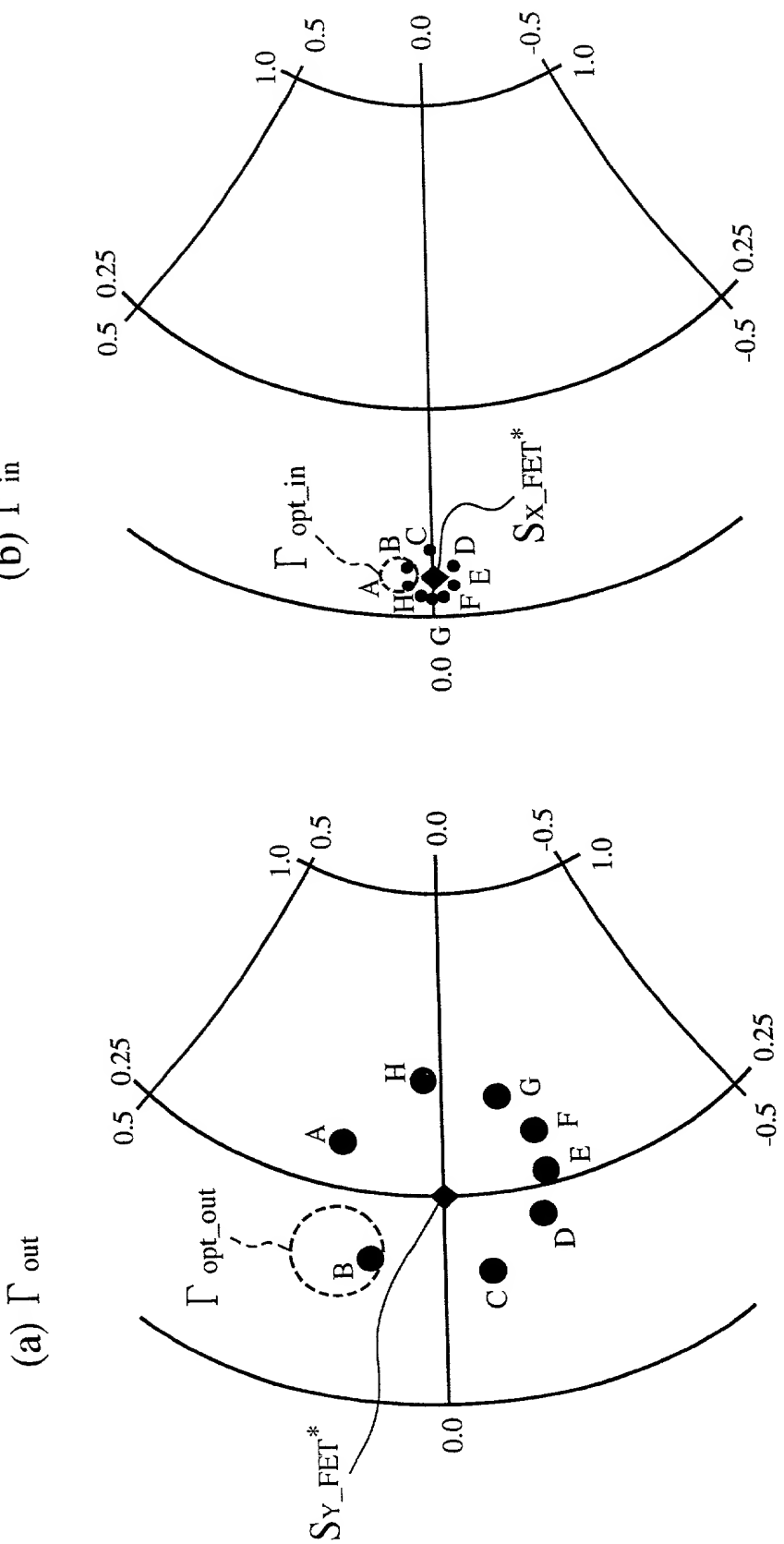

(a) Γ out
(b) Γ in
Γ opt_out
Γ opt_in
SY_FET*
SX_FET*
A
B
C
D
E
F
G
H
0.5
0.25
1.0
0.0
-0.5

FIG.6

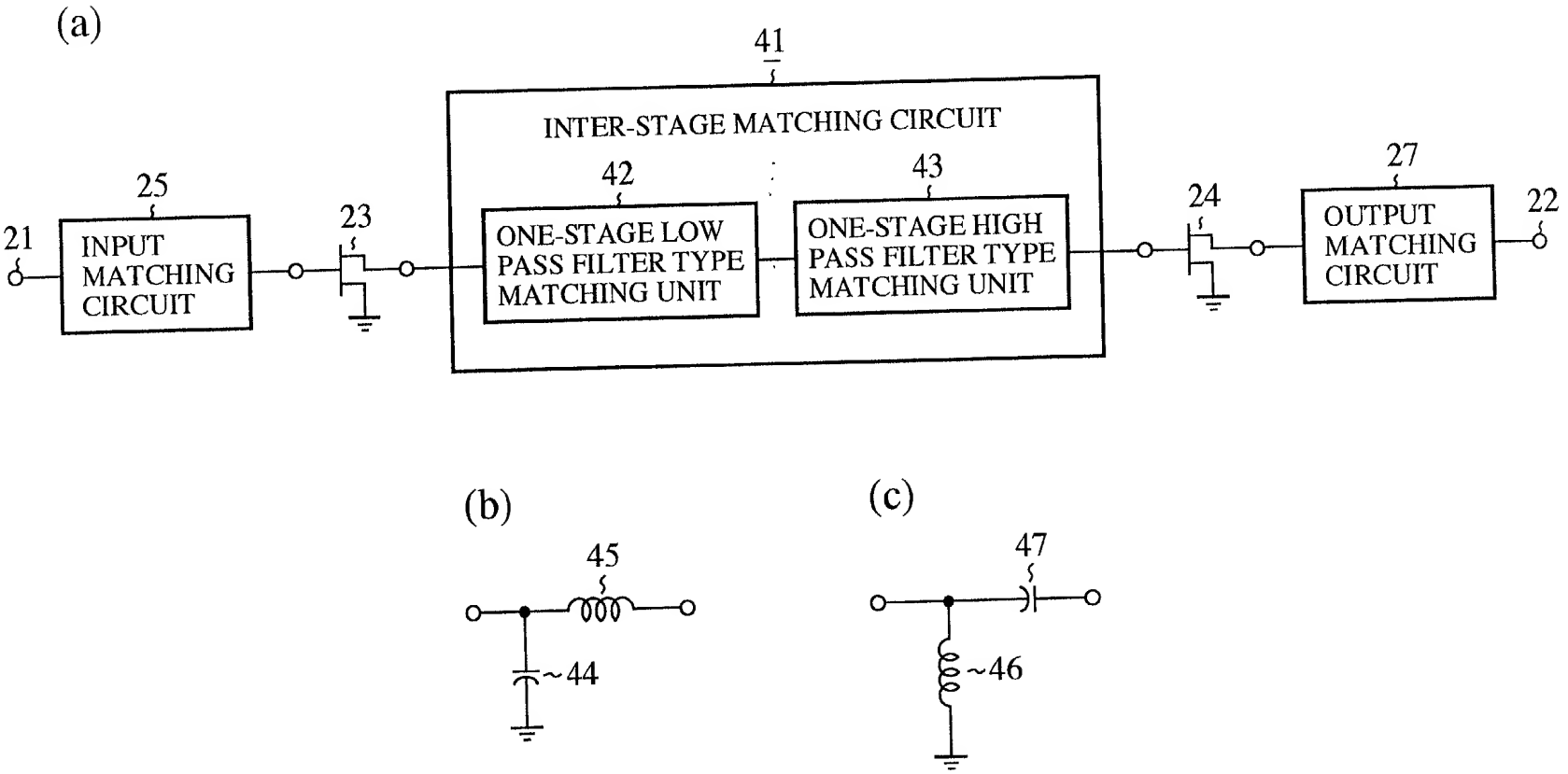


FIG.7

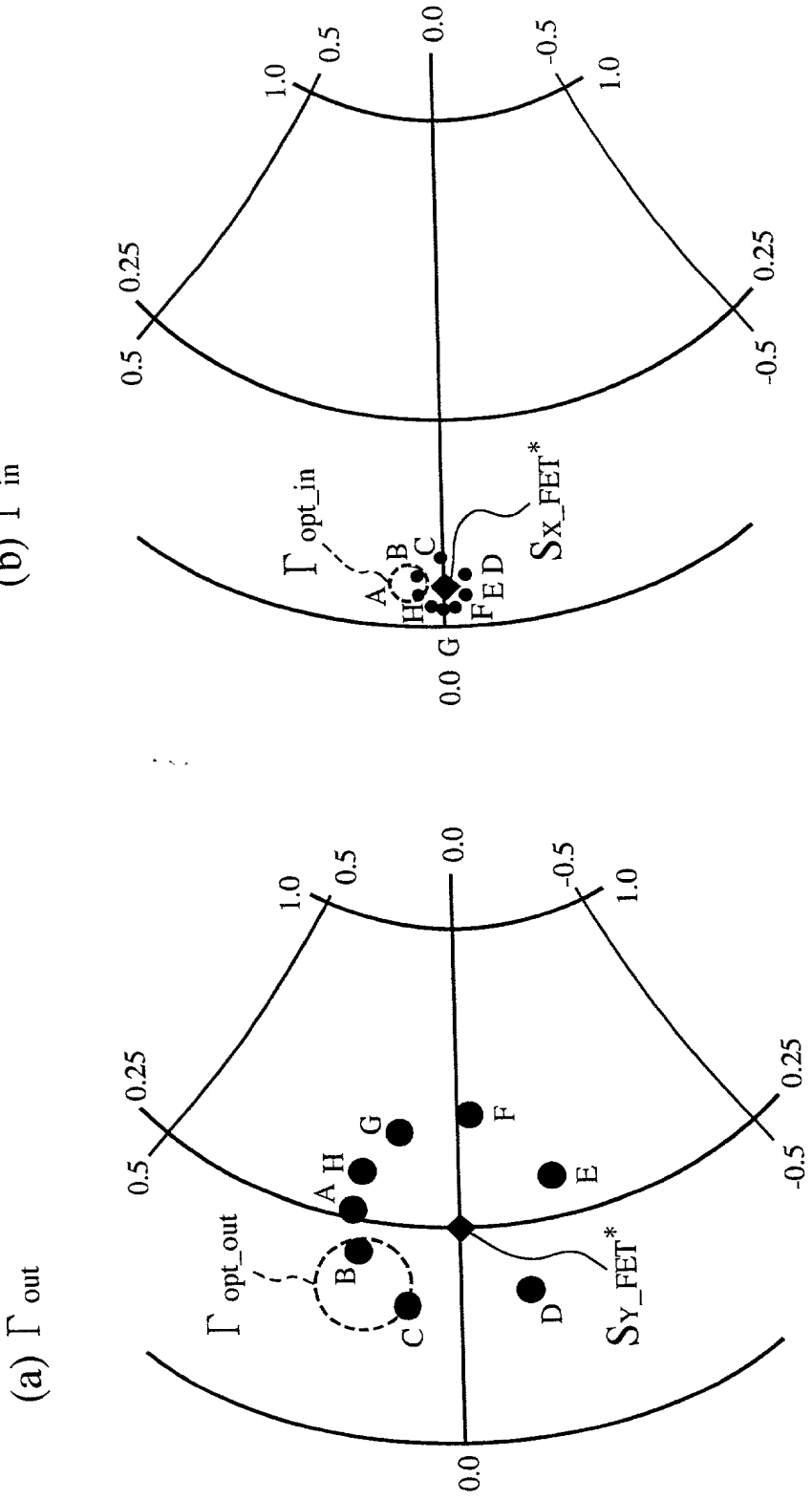

(a) Γ out
(b) Γ in
Γ opt_out
Γ opt_in
Sy_FET*
Sx_FET*
A
B
C
D
E
F
G
H
0.0
0.5
1.0
-0.5
0.25
-0.25

FIG.8

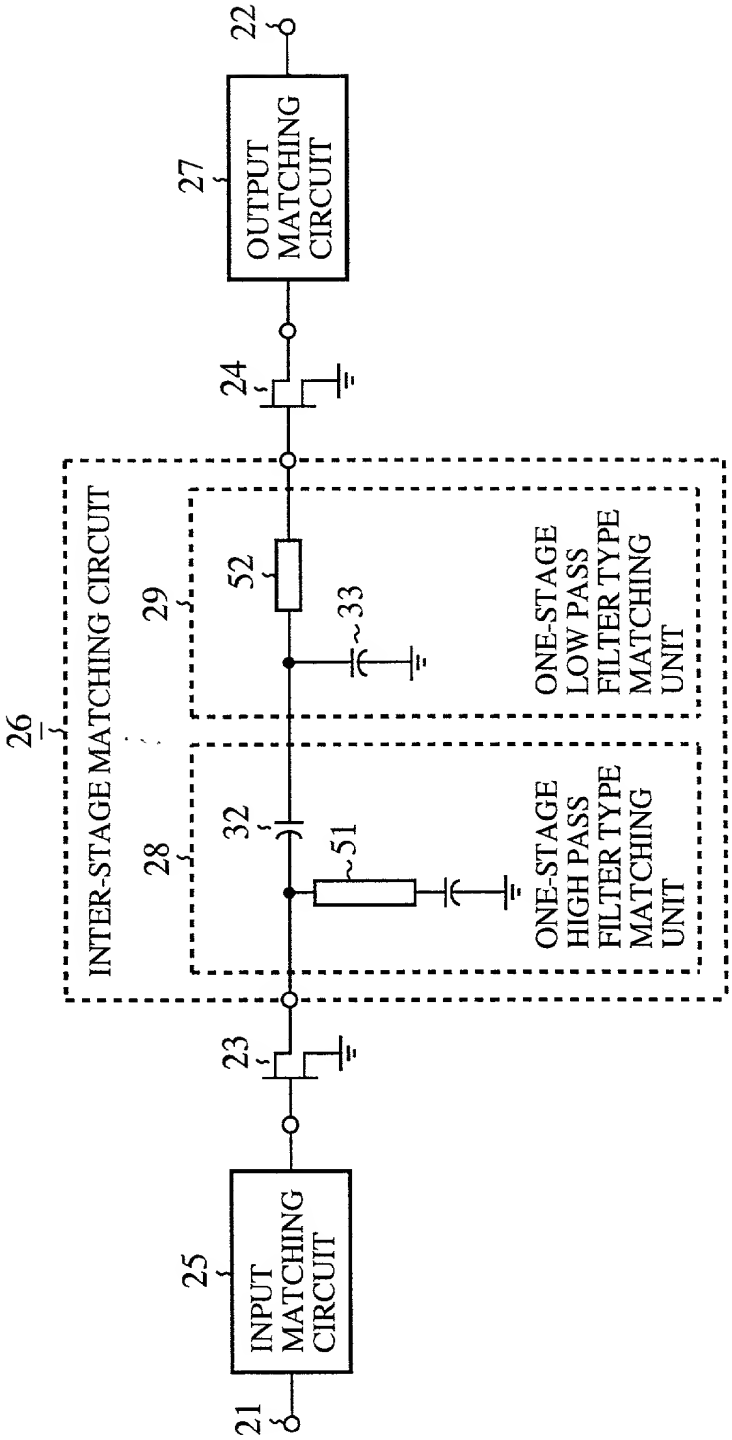
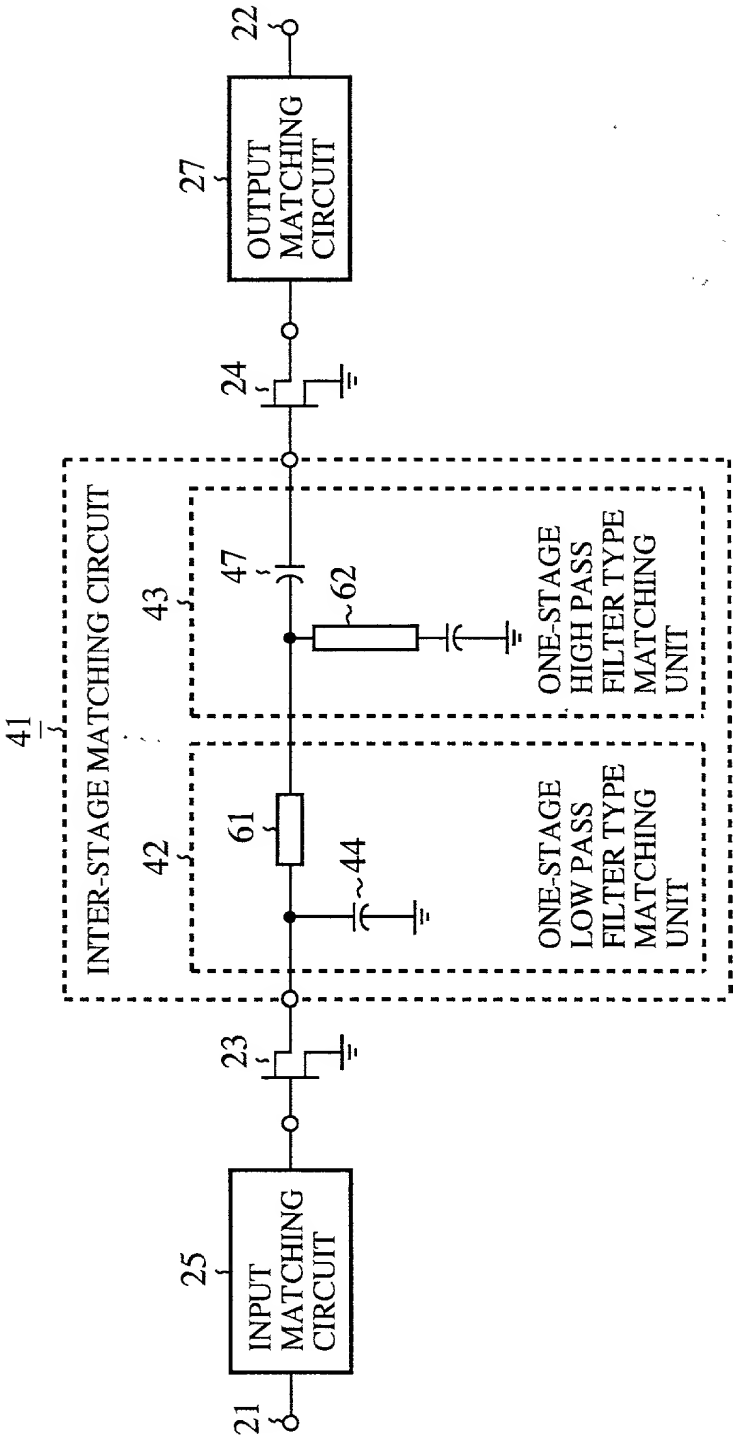

21
INPUT MATCHING CIRCUIT
25
23
26
INTER-STAGE MATCHING CIRCUIT
28
32
51
ONE-STAGE HIGH PASS FILTER TYPE MATCHING UNIT
29
52
33
ONE-STAGE LOW PASS FILTER TYPE MATCHING UNIT
24
27
OUTPUT MATCHING CIRCUIT
22

FIG.9


21
25
INPUT MATCHING CIRCUIT
23
41
INTER-STAGE MATCHING CIRCUIT
42
61
~44
ONE-STAGE LOW PASS FILTER TYPE MATCHING UNIT
43
47
~62
ONE-STAGE HIGH PASS FILTER TYPE MATCHING UNIT
24
27
OUTPUT MATCHING CIRCUIT
22

PTO/SB/106 (8-96)
Approved for use through 9/30/98. OMB 0651-0032
Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

"MULTISTAGE AMPLIFIER"

上記発明の明細書（下記の欄でx印がついていない場合は、本書に添付）は、

the specification of which is attached hereto unless the following box is checked:

☐ __月__日に提出され、米国出願番号または特許協定条約国際出願番号を_____とし、
（該当する場合）_____ に訂正されました。

☒ was filed on February 8, 2000
as United States Application Number or
PCT International Application Number
PCT/JP00/00682 and was amended on
_____ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第３７編第１条５６項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

PTO/SB/106 (8-96)
Approved for use through 9/30/96. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Japanese Language Declaration
(日本語宣言書)

私は、米国法典第３５編１１９条(a)-(d)項又は３６５条(b)項に基き下記の、米国以外の国の少なくとも一ヵ国を指定している特許協力条約３６５(a)項に基ずく国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示しています。

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)
外国での先行出願

Priority Not Claimed
優先権主張なし

(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	☐
(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	☐

私は、第３５編米国法典１１９条(e)項に基いて下記の米国特許出願規定に記載された権利をここに主張いたします。

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Application No.) (出願番号)	(Filing Date) (出願日)

私は、下記の米国法典第３５編１２０条に基いて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約３６５条(c)に基ずく権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第３５編１１２条第１項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願書提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規則法典第３７編１条５６項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365(c) of any PCT international application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of application.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)
(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)

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Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Japanese Language Declaration
(日本語宣言書)

委任状： 私は下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。（弁護士、または代理人の氏名及び登録番号を明記のこと）

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